EE 512: VLSI Lab

1. Parameter extraction for NMOS and PMOS devices.
2. Analysis of Inverter characteristics for arbitrary sizing.
3. Designing of CMOS inverter for a given specifications.
4. Introduction to layout techniques and implementation of inverter in layout.
5. Analysis and designing of NAND logic gate along with the layout.
6. Introduction to progressive sizing and also designing of inverter chains using progressive sizing to improve delay performance.
7. Extraction of integrated resistance and capacitor's parameters
8. Designing of integrated resistor and capacitor for the required values.